



## PATENT ABSTRACTS OF JAPAN

(11) Publication number: **09036362 A**

(43) Date of publication of application: 07.02.97

(51) Int. Cl. **H01L 29/78**

(21) Application number: 07185783

(22) Date of filing: 21.07.95

(71) Applicant: **MITSUBISHI ELECTRIC CORP**

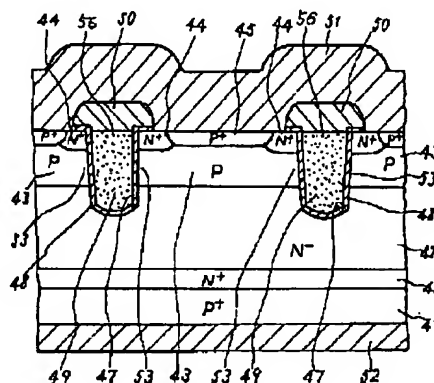
(72) Inventor: **TAKAHASHI HIDEKI**

(54) INSULATED GATE TYPE SEMICONDUCTOR  
DEVICE AND FABRICATION THEREOF

(57) Abstract:

**PROBLEM TO BE SOLVED:** To improve SOA of an insulated gate type semiconductor device by making difficult for a parasitic transistor of an insulated gate type semiconductor device to turn ON.

**SOLUTION:** A parasitic bipolar transistor formed of N<sup>+</sup> emitter region, P base layer and N<sup>-</sup> layer is set difficult to turn ON by providing P<sup>+</sup> semiconductor layer 45 having impurity concentration higher than that of the N<sup>-</sup> emitter region 44 in such a manner that it overlaps with the end part adjacent to the N<sup>+</sup> emitter region 44 of U type IGBT and in contact with the P base region 43 at the bottom part.



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